

REMARKS

Claims 3, 4, 9, and 12-14 are pending in the above-identified application.

Rejection under 35 U.S.C. §102(b) by Chen et al.

Claims 1-4 and 9-12 were rejected under 35 U.S.C. §102(b) as being anticipated by Chen et al. (U.S. Pat. No. 5,045,898). Because claims 1 –2 and 10 –11 are cancelled, their rejections are mooted. The rejections of claims 3, 4, 9, and 12 are respectfully traversed in view of the following remarks. As discussed by the Applicants on page 3, lines 20 – 29, as the channels of transistors becomes shorter, undesirable short channel effects had lead to the reduction of source and drain dopant levels. This reduction, however, produces unacceptably high series resistance between the source and drain. As a result, retrograde doping processes, such as the one disclosed in the Chen reference cited by the Examiner, have been developed to reduce this resistance.

However, note that the retrograde doping disclosed by Chen uses a conventional ion implantation process (to produce a boron implant). See, e.g., Col. 2, lines 28 – 47. Thus, as shown in Figure 3, the resulting boron implant will have a concentration that is uniform laterally throughout the implanted area. In other words, although the boron has a retrograde distribution in a direction normal to the substrate surface, it has a uniform distribution in a direction parallel to the substrate surface.

Such a uniform distribution stands in sharp contrast to the distribution developed by the present invention. For example, consider Applicants' Figure 2, which shows the n-type implants [elements 80] concentrated more toward the center of the channels. Such a non-uniform lateral distribution results from the tilt-type implantation process used to produce the implants, a process neither disclosed nor suggested by the Chen reference.

These differences between the present invention and the Chen reference are reflected in the claims. For example, claim 3 recites a “channel region having a non-uniform concentration of dopant,” wherein the non-uniform concentration “comprises a lateral concentration distribution along the length of the channel that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.” Significant advantages flow from such a distribution. Specifically, if a uniform lateral distribution such as that disclosed in the Chen reference is used instead of the recited distribution, the source and drain regions will be adjacent implants of higher concentration. Thus, larger depletion regions will form, exacerbating short channel effects. By having a non-uniform lateral distribution as recited in claim 3, such short channel effects are minimized.

Note that the same non-uniform lateral distribution is recited in claim 9. Specifically, claim 9 recites a “channel region having a non-uniform concentration of dopant,” wherein the “non-uniform concentration comprises a lateral concentration distribution along the length of the channel that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.” Accordingly, both claims 3 and 9 are patentable over the Chen reference. Because claims 4 and 12 depend upon claims 3 and 9, respectively, they are patentable for the same reasons.

New claims 13 and 14, being ultimately dependent upon claim 9, are also patentable for the reasons given above.

In addition, Applicants have corrected a few typographical errors in the specification.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

CONCLUSION

For the above reasons, Applicants believe the pending claims are now in condition for allowance and a notice of allowance is respectfully requested.

If the Examiner has any questions regarding the application, the Examiner is invited to call the undersigned Attorney at (949) 718-5200.

EXPRESS MAIL LABEL NO:

EV 004868366 US

Respectfully submitted,



Jon Hallman
Attorney for Applicants
Reg. No. 42,622

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
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FAX (408) 453-7979

EXHIBIT A

3.(amended) A [The] memory array [of claim 2,] comprising a plurality of floating gate transistors connected in series, each floating gate transistor having formed, in a well of a substrate, a source and a drain region and a channel region separating said source and drain regions, said channel region having a non-uniform concentration of dopant; wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction from the surface of the substrate, and wherein said non-uniform concentration comprises a lateral concentration distribution along the length of the channel that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.

9. An [isolated gate floating gate NMOS] transistor comprising, in a well structure of a substrate, a source and a drain region and a channel region separating the source and the drain region, said channel region having a non-uniform concentration of dopant, wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction away from the surface of the substrate, and wherein said non-uniform concentration comprises a lateral concentration distribution along the length of the channel that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.

EXHIBIT B

The paragraph beginning on page 5, line 4 has been amended as follows:

In one embodiment, select transistor 12 has an amorphous poly-silicon ("poly") gate 44s (formed as further explained below) and separated from a channel region 70 between drain region 40 and source region 60 by an oxide layer 50 which may be, for example, 168 Å thick. Select transistor 12's poly gate 44s is covered by a thin tungsten silicide layer 58s.

The paragraph beginning on page 5, line 11 has been amended as follows:

Oxide layer 50 may be thermally grown using a dry oxidation process at about 1050° C[.] to a thickness of about 148 Å. A photoresist mask is then used to pattern for an etching step that exposes the substrate outside of the select transistors (e.g., select transistor 12). Then, a film of about 87 Å of oxide is formed as tunnel oxide 52 using a dry thermal oxidation process at about 1050° C. Due to the slower growth rate on oxide layer 50, oxide layer 50 only increases about 20 Å to a thickness of about 168 Å.

The paragraph beginning on page 6, line 15 has been amended as follows:

A retrograde distribution of dopant is then introduced by ion implantation into the channel regions 72, 74 and 76, while channel region 70 under select transistor 12 is masked by photoresist. The retrograde distribution of dopant is accomplished by implanting an n-type dopant (e.g., arsenic) at a tilt implant angle of, for example, 45° to vertical. Other tilt angles may also be suitable. The implantation can be made with a "batch-type" machine or with a

single-wafer machine. In a batch-type machine, the wafer is rotated during the tilt implantation process. In a single-wafer machine, the implantation is done with a zero degree twist and a 180 degree twist (i.e., a[n] tilt implantation through one side of source/drain regions 60, 62, and 64, followed by a like tilt angle implantation deposition through the source/drain regions 62, 64 and 66). Implantation energies between 80 and 110 KeV are suitable, forming resulting dopant concentrations of about 2×10^{-12} to 8×10^{-13} atoms per cm^2 .

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SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979